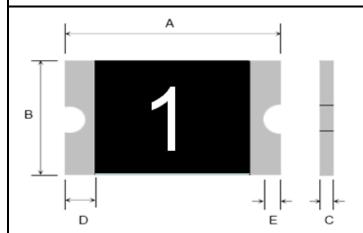
JK-SMD0805-010 PPTC DEVICES

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Terminal pad materials: Tin-Plated Nickle-copper

Terminal pad solderability: Meets EIA specification RS 186-9E and ANSI/J-STD-002 Category 3.

Marking: Part identification 1=010

Table1:DIMENTION(Unit:mm)

Model	Marking	A		В		С		D	Е
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Min.
JK-SMD0805-010	1	2.00	2.20	1.20	1.50	0.50	1.00	0.20	0.10

Table2:PERFORMANCE RATINGS:

Model	Marking	V _{max} (Vdc)	I _{max} (A)	I _{hold} @25℃ (A)	I _{trip} @25℃ (A)	P _d Typ (W)	Maximum Time To Trip		Resistance		
							Current	Time	Ri_{min}	Ri_{typ}	$R1_{max}$
				(A)	(A)	(W)	(A)	(Sec)	(Ω)	(Ω)	(Ω)
JK-SMD0805-010	1	15.0	100	0.10	0.30	0.50	0.5	1.50	1.000	2.500	6.000

Table3:Test Conditons and Standards

Item	Test Conditon	Standard		
Initial Resistance	25℃	$1.000{\sim}6.000\Omega$		
$ m I_H$	25°C, 0.10A, 60min	No Trip		
Ttrip	25℃, 0.5A	≤1.5s		
Trip endurance	15V, 100A, 60min	No arcing or burning		

Operating Temperature: -40°C TO 85°C

Packaging: Bulk ,5000pcs per bag

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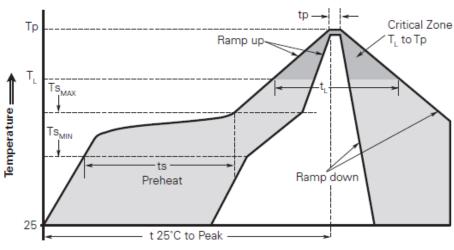
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Solder reflow conditions



Reflow Profile Time

Profile Feature	Pb-Free Assembly			
Average ramp up rate (Ts _{MAX} to Tp)	3°C/second max.			
Preheat				
 Temperature min. (Ts_{MIN}) 	150°C			
 Temperature max. (Ts_{MAX}) 	200°C			
 Time (ts_{MIN} to ts_{MAX}) 	60-120 seconds			
Time maintained above:				
• Temperature (T _L)	217°C			
• Time (t _L)	60-150 seconds			
Peak/Classification temperature (Tp)	260°C			
Time within 5°C of actual peak temperatur	e			
Time (tp)	30 seconds max.			
Ramp down rate	3°C/second max.			
Time 25°C to peak temperature	8 minutes max.			

Note: All temperatures refer to topside of the package, measured on the package body surface.

- Recommended reflow methods: IR, vapor phase oven, hot air oven, N2 environment for lead-free.
- Devices are not designed to be wave soldered to the bottom side of the board.
- Recommended maximum paste thickness is 0.25mm (0.010inch).
- Devices can be cleaned using standard industry methods and solvents.
- Soldering temprature profile meets RoHs leadfree process.

Notes: If reflow temperatures exceed the recommended profile, devices may not meet the performance requirements

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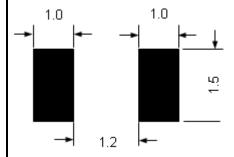
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Recommended pad layout (mm)



WARNING

- · Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
- · PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
- · Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
- · Use PPTC with a large inductance in circuit will generate a circuit voltage (L di/dt) above the rated voltage of the PPTC.
- · Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
- · Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices.PPTC SMD can be cleaned by standard methods.
- · Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profilecould negatively impact solderability performance of our devices.

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