SPECIFICATION

Customer:

Model Name: SAT035TM54DHR1-A0-01

SPEC NO.:

Date:

Version:

视安通集团SAT GROUP

■ Preliminary Specification

□ Final Specification

Approved by	Comment

Approved by	Reviewed by	Prepared by
视安通 2014.12.01 吴金荣		

Record of Revision

Version	Revise Date	Page	Content
Pre-spec.A	2014/12/01		Initial Release

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1. General Specifications

No.	Item	Specification	Remark
1	LCD size	3.5 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	320 × 3(RGB) ×240	
4	Display mode	Normally White, Transmissive	
5	Pixel pitch	0.219(H) X 0.219(V) mm	
6	Active area	70.08(H) X 52.56(V) mm	
7	Outline dimensions	76.9(H) X 63.9(V) X 3.0(D) mm	
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	RGB/CCIR656/601	
11	Backlight Power consumption	TBD	
12	Panel Power consumption	TBD	
13	Weight	TBD	

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2. Pin Assignment

FPC Connector is used for the module electronics interface. The recommended model is FH12A-54S-0.5SH manufactured by Hirose

No	Symbol	I/O	Description	Remarks
1	LED_Cathode	P	LED_Cathode	
2	LED_Cathode	P	LED_Cathode	
3	LED_Anode	P	LED_ Anode	
4	LED_Anode	P	LED_Anode	
5	NC	--	No Connection	
6	NC	--	No Connection	
7	NC	--	No Connection	
8	RESET	I	Reset	
9	SPENA	I	Serial Port Data Enable Signal	
10	SPCK	I	SPI Serial Clock	
11	SPDA	I	SPI Serial Data Input	
12	DATA0	I	Data Bus	
13	DATA1	I	Data Bus	
14	DATA2	I	Data Bus	
15	DATA3	I	Data Bus	
16	DATA4	I	Data Bus	
17	DATA5	I	Data Bus	
18	DATA6	I	Data Bus	
19	DATA7	I	Data Bus	
20	DATA8	I	Data Bus	
21	DATA9	I	Data Bus	
22	DATA10	I	Data Bus	
23	DATA11	I	Data Bus	
24	DATA12	I	Data Bus	
25	DATA13	I	Data Bus	
26	DATA14	I	Data Bus	
27	DATA15	I	Data Bus	
28	DATA16	I	Data Bus	
29	DATA17	I	Data Bus	
30	DATA18	I	Data Bus	
31	DATA19	I	Data Bus	
32	DATA20	I	Data Bus	

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33	DATA21	I	Data Bus	
34	DATA22	I	Data Bus	
35	DATA23	I	Data Bus	
36	HSYNC	I	Horizontal Synchronous Signal	
37	VSYNC	I	Vertical Synchronous Signal	
38	DOTCLK	I	Data Clock	
39	NC	--	No Connection	
40	NC	--	No Connection	
41	VDD	P	Digital Power Supply	
42	VDD	P	Digital Power Supply	
43	NC	--	No Connection	
44	NC	--	No Connection	
45	NC	--	No Connection	
46	NC	--	No Connection	
47	NC	--	No Connection	
48	NC	--	No Connection	
49	NC	--	No Connection	
50	NC	--	No Connection	
51	NC	--	No Connection	
52	DEN	I	Data Enabling Signal	
53	GND	P	Ground	
54	GND	P	Ground	

I: input, O: output, P: Power

Note1: I/O definition:

I----Input O----Output P----Power/Ground

Note2: Interface controlled by SPI, please refer to the SPI command list.

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Mode	D(23:16)	D(15:8)	D(7 : 0)	HSYNC	VSYNC	DEN
CCIR 656	DATA(23:16)	GND	GND	NC	NC	NC
CCIR 601	DATA(23:16)	GND	GND	HSYNC	VSYNC	NC
8 Bit RGB	DATA(23:16)	GND	GND	HSYNC	VSYNC	NC for HV Mode
						DEN for DEN Mode
24 Bit RGB	DATA(23:16)	DATA(15:8)	DATA(7:0)	HSYNC	VSYNC	NC for HV Mode
						DEN for DEN Mode

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Supply voltage	VCIP	-0.3	5.0	V	
Supply voltage	V1–V6	-0.3	VDDA+0.3	V	
Logic Supply voltage	VCI	-0.5	5.0	V	
Analog Supply voltage	VDDA	-0.5	7.5	V	
	V_{GH}-V_{GL}	-0.3	25	V	
Operation Temperature	T_{OP}	-20	70	℃	
Storage Temperature	T_{ST}	-30	80	℃	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

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3.1.1. Typical Operation Conditions

(Test Condition: VCI=VCIP=3.3V, VDDA=5.0V, VSS=GNDA=VSSP=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply Voltage	VCI	3.0	3.3	3.6	V	
I/O power supply	VDDIO	VDD	3.3	3.6	V	
Pump circuits supply	VCIP	3.0	3.3	3.6	V	
Low power supply	VDD	1.6	1.8	2.0	V	
Low Level Input Voltage	Vil	VSS	-	0.2xVDDIO	V	Digital input pins TA=25℃
High Level Input Voltage	Vih	0.8xVDDIO	-	VDDIO	V	Digital input pins TA=25℃
Input Leakage Current	Ii	-	-	±1	μA	Digital input pins
High Level Output Voltage	Voh	VDDIO-0.4	-	VDDIO	V	Digital output pins; Ioh=400μA
Low Level Output Voltage	Vol	VSS	-	VSS+0.4	V	Digital output pins; Iol=-400μA
2xVCI pump output level	VINT1	5.2	5.5	5.8	V	VCIP=3.3V, w/o panel loading
Analog power voltage	VDDA	4.5	5.0	VINT1-0.3	V	Analog circuit power from Power Block
VCOMAC output level	VCOMAC	4.6	-	VINT1-0.3	V	By VCSL[2:0] setting VCOMAC=$V_{(VCSL[3:0])}$±100mV
VCOMDC output level	VCOMDC	1.0	-	2.26	V	By VCDCSL[5:0] setting VCOMDC= $V_{(VCDCSL[5:0])}$±50mV
Positive power supply	VGH	14.5	15	15.5	V	Gate driver load + procard load
Negative power supply	VGL	-10	-8	-6	V	Gate driver load + procard load
Base drive current	IDRV	-	-	10	mA	VCIP=3.3V, DRV=0.7V
DRV output voltage	VDRV	VSS+0.1	-	VCI-0.1	V	
Feed back voltage	VFB	0.55	0.6	0.65	V	DC/DC operating, VBL current=20mA
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V~0.5V & VDDA-0.5V~VDDA-0.1V
			±15	±25	mV	Vo=0.5V~VDDA-0.5V
Low-Level Output Current of VCOMOUT	IOLF	-	-10	-	mA	Force VCOMAC=6.0V VCOMOUT output=0V V.S 0.9V
High-Level Output Current of VCOMOUT	IOHF	-	10	-	mA	Force VCOMAC=6.0V VCOMOUT output=6.0V V.S 5.1V
Source Low-Level Output Current	I_{OLS}	-	-30	-	μA	Son=Vo V.S. (Vo+0.9)
Source High-Level Output Current	I_{OHS}	-	30	-	μA	Son=Vo V.S. (Vo-0.9)
Gate Low-Level Output Current	IOLG	-	-250	-	μA	GOn; Vo=VGL V.S. (VGL+0.5)
Gate High-Level Output Current	IOHG	-	250	-	μA	GOn; Vo=VGL V.S. (VGH-0.5)
Chip Stand-by Current	Idds	-	15	50	μA	STBYB="0", all function are shutdown, CLKIN/VSD/HSD halted
Chip Operating Current	Idda	-	10	-	mA	No load, CLKIN=27MHz, Fld=15KHz

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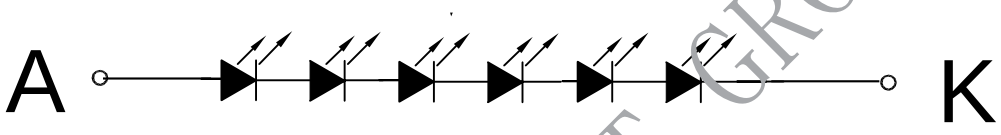
3.1.2. Backlight Driving Conditions (6 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	17.4	19.8	21	V	Note 1
Current for LED backlight	IL	15	20	25	mA	
Luminance (on the module surface,BM-7)		360	410	-	cd/m^2	
LED life time	-	20,000	-	-	Hr	Note 2



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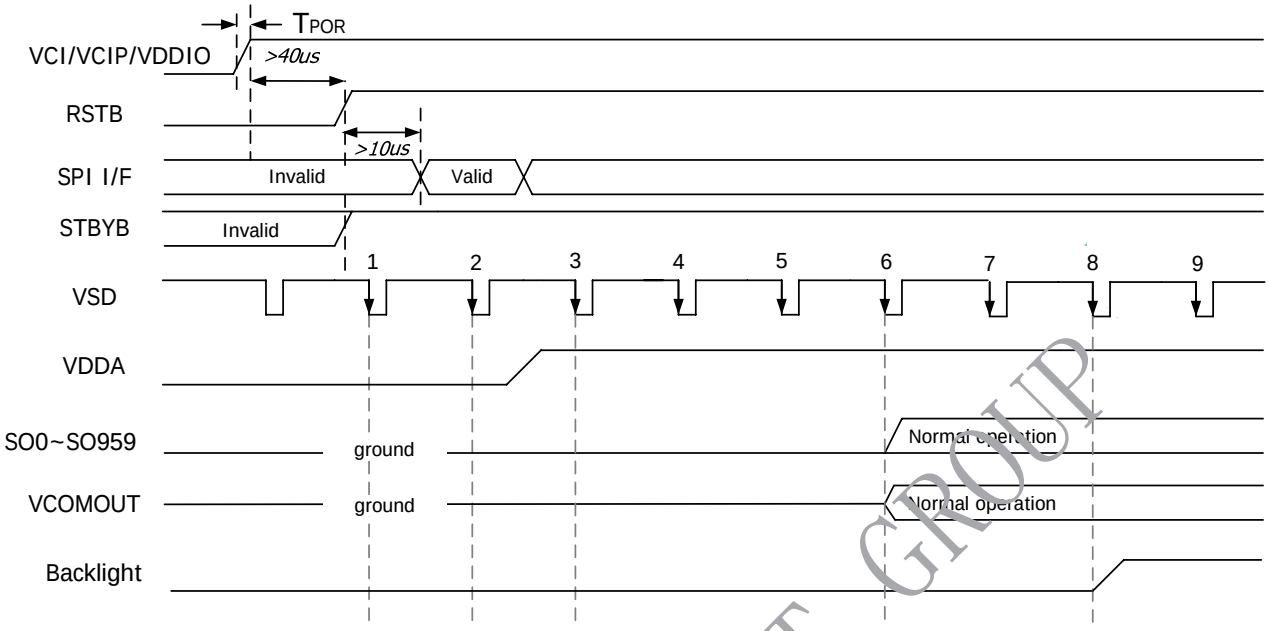
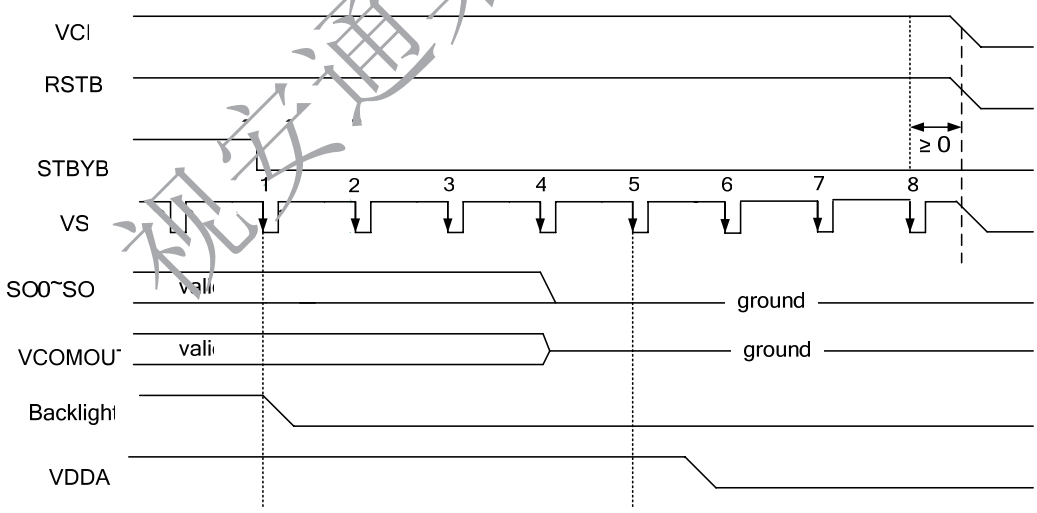
3.2. Power Sequence

3.2.1. Power-On Timing Sequence



3.2.2 Power-Off Timing Sequence



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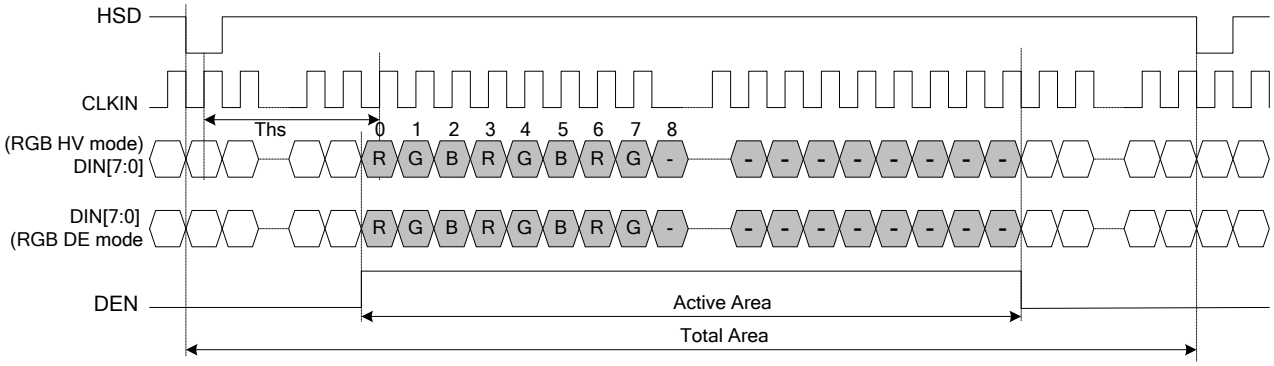
3.3. Timing Characteristics

3.3.1 Input Data Format

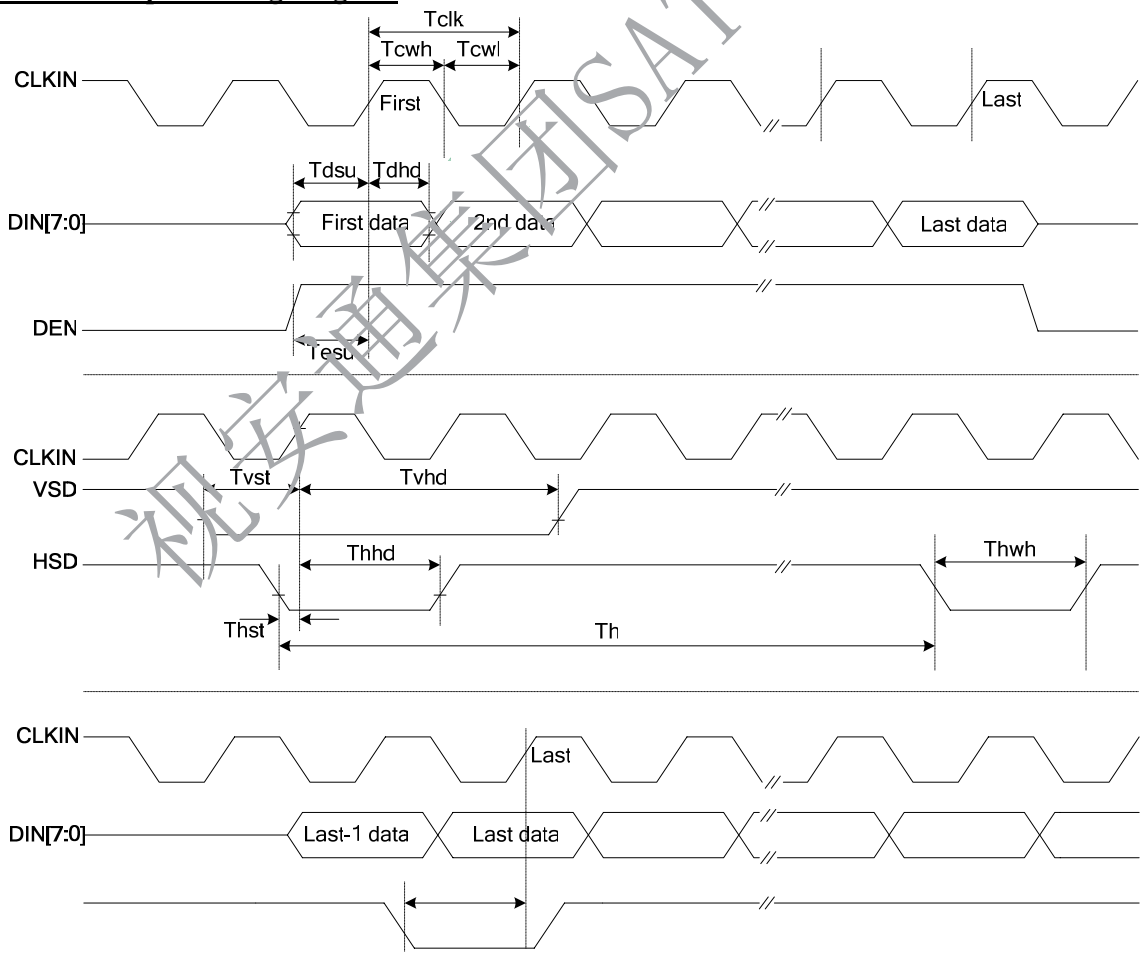
Input Data Format



Input Format	Format Standard	CLKIN(MHz)	HSD(CLKIN)	Total Area (CLKIN)	Active Area (CLKIN)	Note
8bit RGB	8bit RGB	27	1	1716	960	960×240
24bit RGB	24bit RGB	6.4	1	408	320	

3.3.2.Time Diagram

Clock and Data Input Timing Diagram



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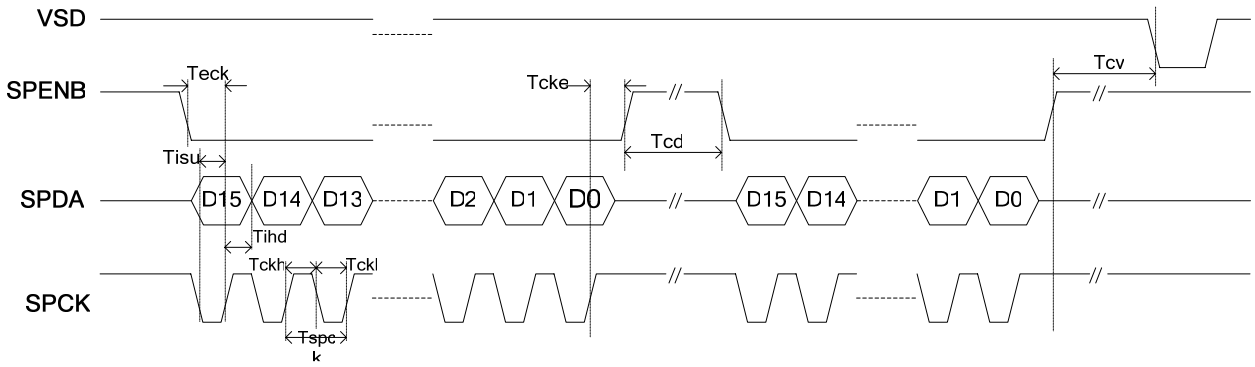
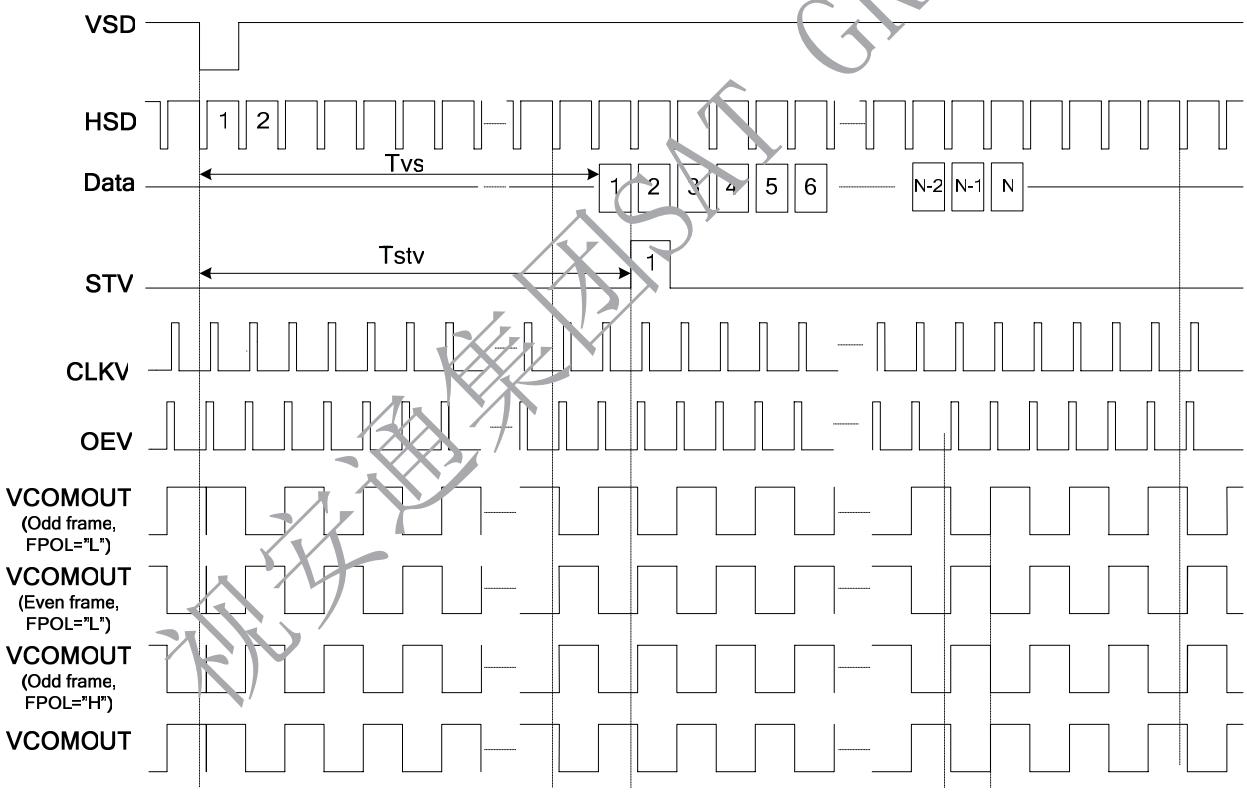
3-Wire Timing Diagram



Vertical Timing Diagram (HV Mode)



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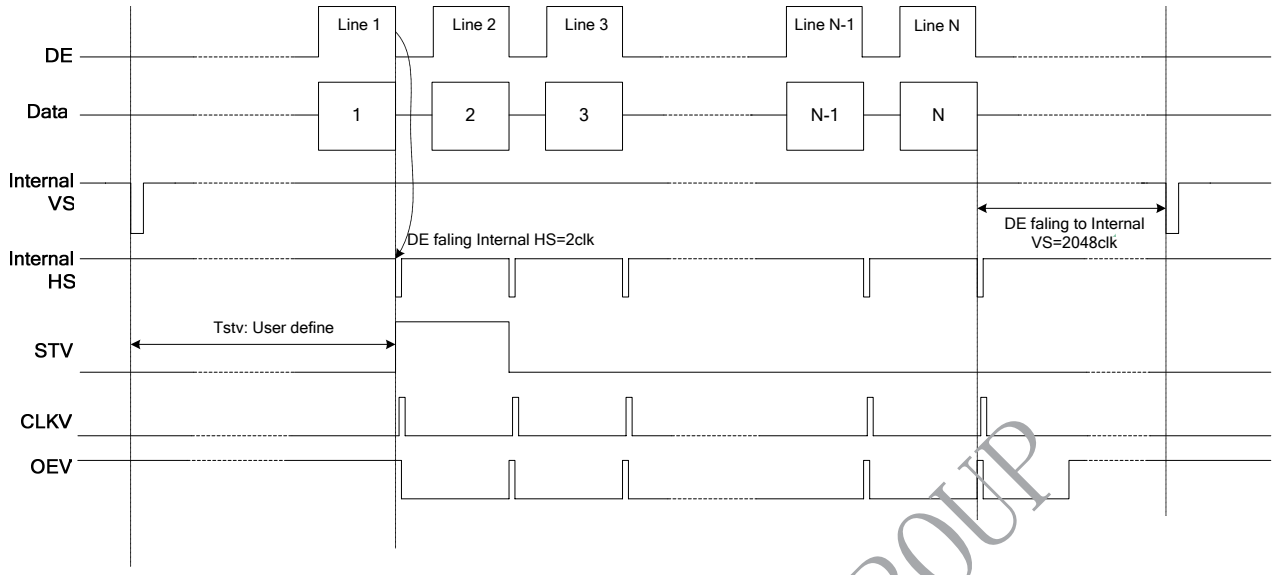
Vertical Timing Diagram (DE Mode)



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3.3. Timing

8 Bit RGB 960 CH Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	35	70	255	CLKIN	DDLY=70,Offset=0(fixed)

24 Bit RGB Mode (@ SEL[3:0]=1100 or 1101)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	6.1	6.4	8.0	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	125	156	164	ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	40	70	255	CLKIN	DDLY=70,Offset=0(fixed)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System Operation Timing						
VDD power source slew time	T_{POR}			1000	us	From 0V to 90% VDD
RSTB active pulse width	T_{RSTB}	40			us	VDD=3.3V
Input Output Timing						
CLKIN clock time	Tclk	-		35.7	ns	Please refer to timing table(P25)
HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD width	Thwh	1	-	-	CLKIN	
VSD width	Tvwh	1	-	-	Th	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data set-up time	Tdsu	12	-	-	ns	DIN[23:0] to CLKIN
Data hold time	Tdhd	12	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	Tesd	12	-		ns	DEN to CLKIN
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@CIR601/8bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Source output stable time 1	Tst	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	Tgst	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	Tcst	-	4	8	us	96% final, CL=33nF, RL=100ohm
3-wire serial communication AC timing						
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty	Tscdut	40	50	60	%	Tckh/Tspck
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tssw	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENA to VSD	Tcv	1	-	-	us	
SPENB input setup time	Teck	150	-	-	Ns	
SPENB input hold time	Tcke	150	-	-	ns	

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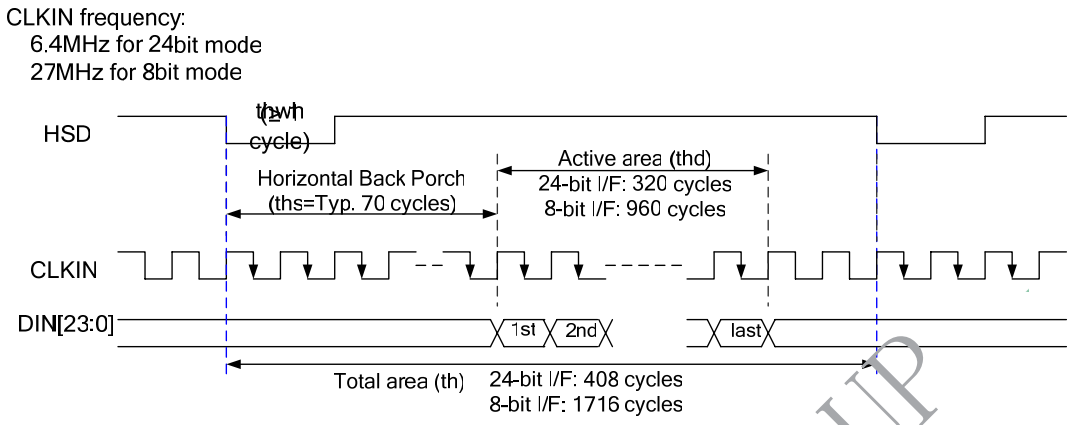
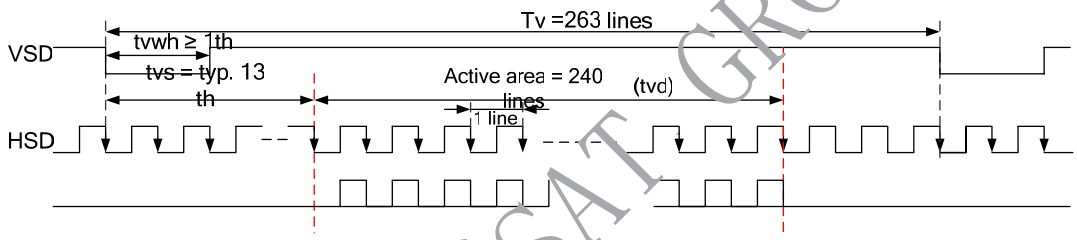
RGB (NTSC) input timing

(1) HV mode timing: DE signal is not necessary, host float this pin.

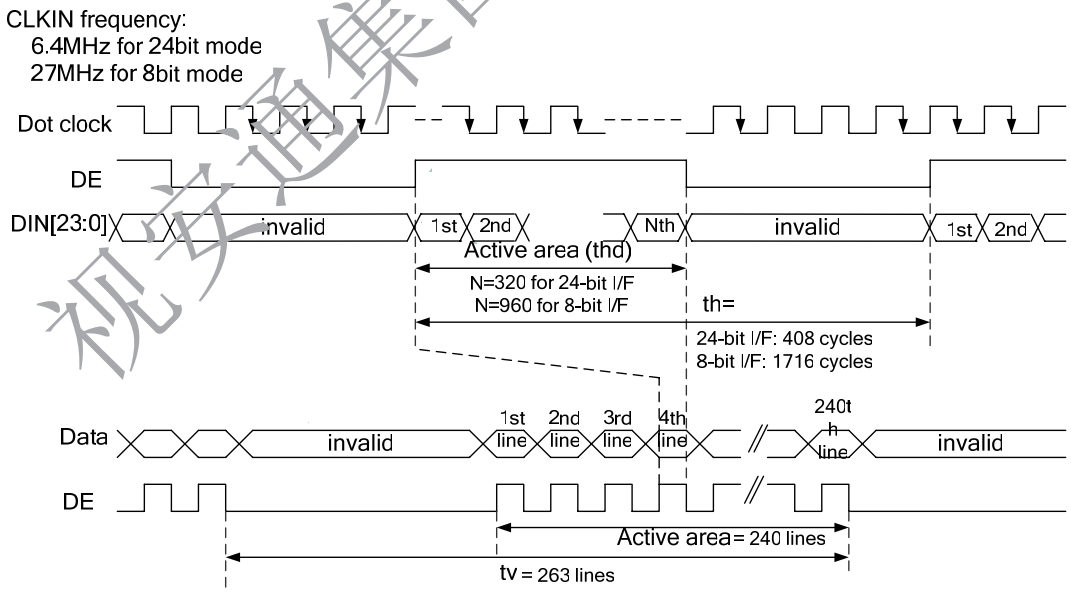
Horizontal:



Vertical:



(2) DE mode: Hsync and Vsync are not needed in DE mode, host float these pins.



Notes:

(1) both CLKIN, HSD, VSD and DE supports active polarity selection. In the diagrams above, the VSD and HSD is low active, CLKIN samples data at negedge, DE is high active, and however, other kinds of polarity of these signals are also supported.

(2) signal relationship timing specification please refers the reference datasheet.

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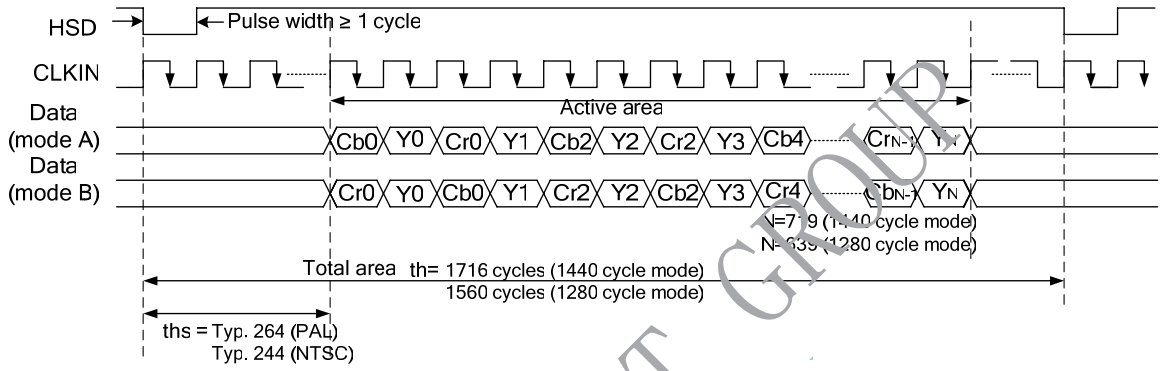
CCIR601 input timing

Features of the CCIR601 supported by this chip:

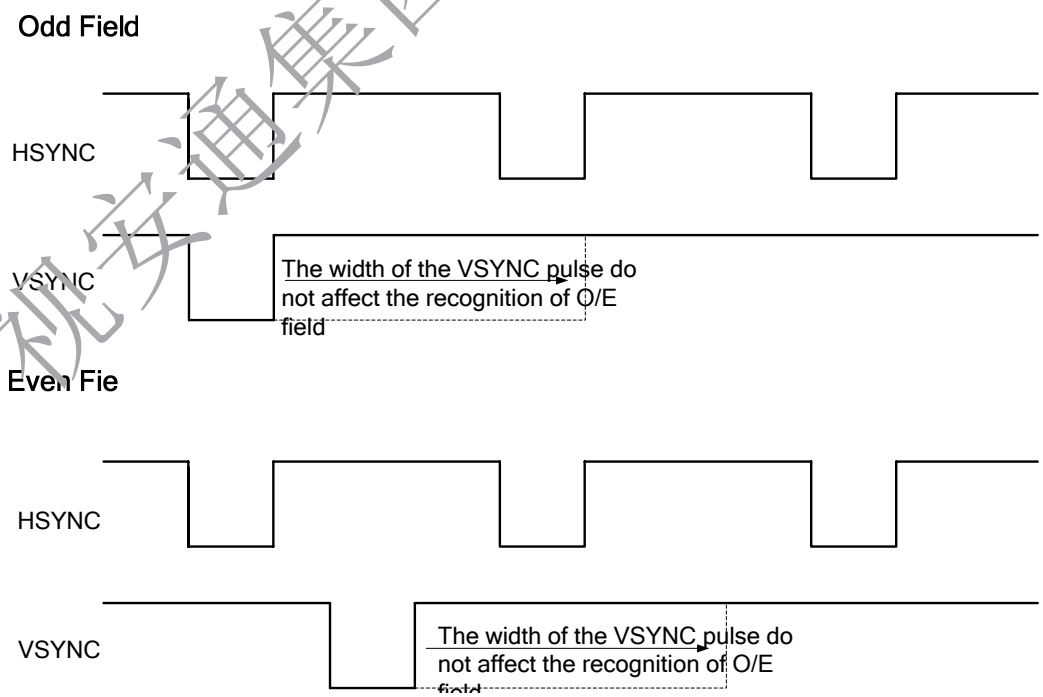
(1) only 8-bit I/F supported
(2) Both PAL and NTSC support. For PAL, both 280 and 288 lines supported
(3) Both 1440 and 1280 horizontal cycles are supported
(4) For all supported CCIR601 input format, the data sequence can be two types: mode A is Cb/Y/Cr/Y, mode B is Cr/Y/Cb/Y

Horizontal signal:

CLKIN frequency:
24.54MHz for 1280-cycle mode
27MHz for 1440-cycle mode



For CCIR601, 1 image frame = 1 odd field + 1 even field
The odd/even filed is recognized by the inter relationship of Hsync and Vsync signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition



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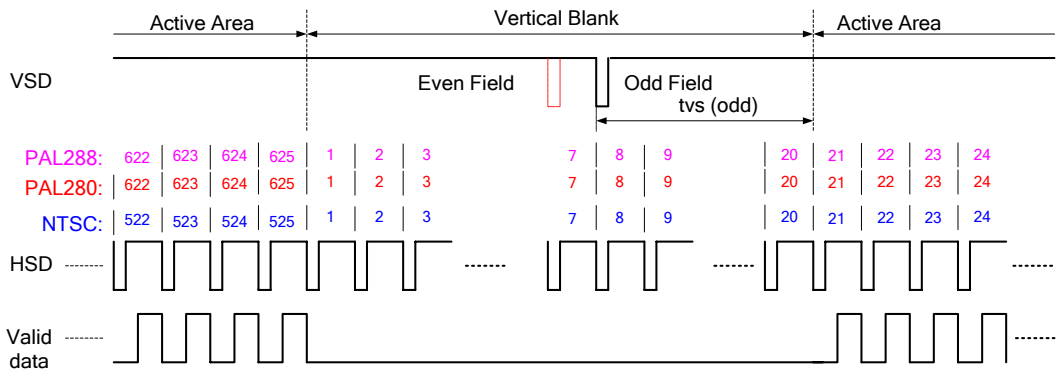
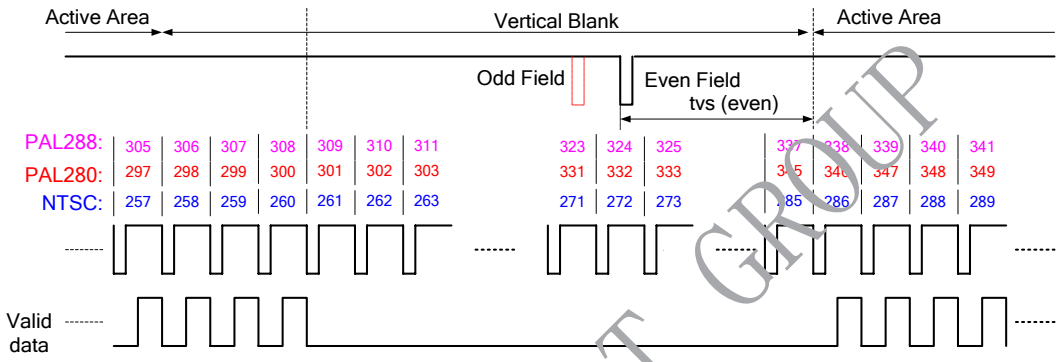
Vertical signal:



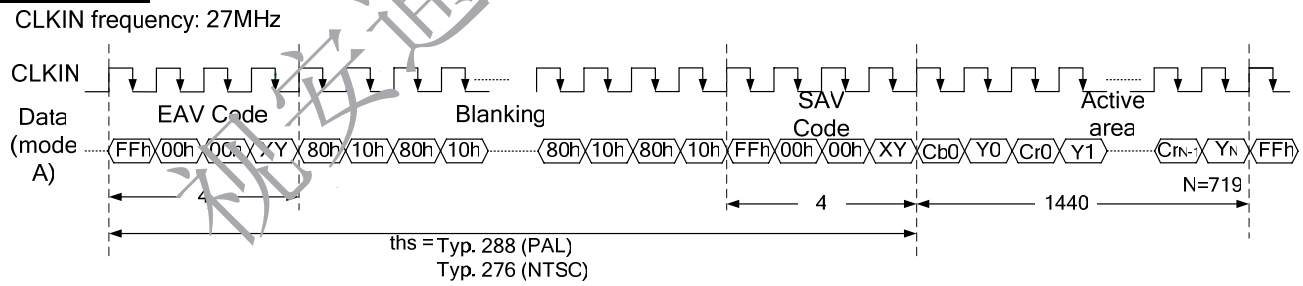


NTSC mode: active area=240 lines; PAL 280 mode: active area=280 lines; PAL 288 mode: active area=288 lines.

CCIR656 input timing

The CCIR656 use the YUV color encoding too. The difference of CCIR656 is that sync signals are embedded into the code stream. By this mode, VSD, HSD, DEN signals are not needed.

Horizontal:



EAV/SAV Format:

the "XY" byte in EAV/SAV plays a critical role for synchronization:

XY	B7	B6	B5	B4	B3	B2	B1	B0
EAV	1	F	V	H	Protection bits by ITU 656			
SAV	1	F	V	H	Protection bits by ITU 656			

F: Field bit. This is for vertical timing. F=0 indicates this is the line of the 1st field (odd field). F=1 indicates this is the line of the 2nd field (even field).

V: Vertical blanking bit. This is for vertical timing. V=1 indicates vertical blanking lines, V=0 indicates an active video line.

H: Horizontal recognizing bit. H=0: SAV, H=1: EAV.

Vertical:

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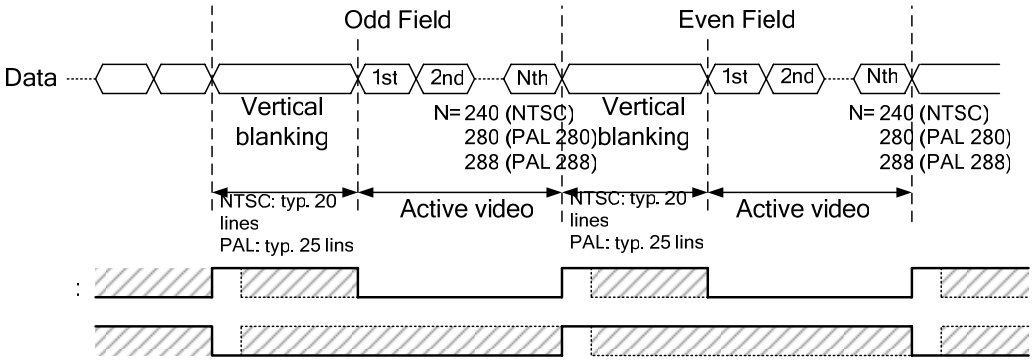

3.4.Registers Table

Following table list the default 3-Wire control registers and bit name definition for NV3035C. Refer to the next section for detail register function description, please.

NV3035C 3-Wire Control Register List (Default)

3-Wire Registers		Register Description		
D[15:10]	**Name**	**Init.**	**R/W**	**Function Description**
000000b	R00	03h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	8Ch	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001011b	R0B	88h	R/W	R/B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	2bh	R/W	VCOMDC Level Control Register
001111b	R0F	A5h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level Control Register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
011101b	R1D	00h	R/W	OTP operation control register
011110b	R1E	00h	R/W	OTP operation control register
011111b	R1F	00h	R/W	OTP operation control register

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NV3035C 3-Wire Register Bit Definition (Default)

3-Wire Control Register Bit Map								
Reg.	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
R00	PAT3	PAT2	PAT1	PAT0	PWMPDB	X	STBYB	RESETB
R01	X	X	X	SWD2	SWD1	SWD0	DITHB	CFTYP
R02	SKIPMOD	HDNC1	HDNC0	X	FPOL	VSET	UPDN	SHLR
R03	DENPOL	CLKPOL	HSDPOL	VSDPOL	SEL3	SEL2	SEL1	SEL0
R04	DDLY7	DDLY6	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R05	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R07	FRAD1	FRAD[0]	INVSL[1]	INVSL[0]	PAL	PALM		AVGY
R08	X	X	X	CON4	CON3	CON2	CON1	CON0
R09	X	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
R0A	HUE[3]	HUE[2]	HUE[1]	HUE[0]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
R0B	SCONB1	SCONB0			SCONR1	SCONR0		
R0C	X	X	SBRIR5	SBRIR4	SBRIR3	SBRIR2	SBRIR1	SBRIR0
R0D	X	X	SBRIB5	SBRIB4	SBRIB3	SBRIB2	SBRIB1	SBRIB0
R0E	X	OTP_BYPS	VCDCSL5	VCDCSL4	VCDCSL3	VCDCSL2	VCDCSL1	VCDCSL0
R0F	VGLSL1	VGLSL0	VGHSL1	VGHSL0	VCACSL3	VCACSL2	VCACSL1	VCACSL0
R10	X	X	X	GAMEN	X	V2GAM2	V2GAM1	V2GAM0
R11	X	X	V4GAM2	V4GAM1	V4GAM0	V3GAM2	V3GAM1	V3GAM0
R12	X	X	V6GAM2	V6GAM1	V6GAM0	V5GAM2	V5GAM1	V5GAM0
R1D	PDIN[7]	PDIN[6]	PDIN[5]	PDIN[4]	PDIN[3]	PDIN[2]	PDIN[1]	PDIN[0]
R1E	PPROG	PSWSL	PWE	POR	PTM[1]	PTM[0]	PA[1]	PA[0]
R1F								OTPSEL
R20							WNSEL[1]	WNSEL[0]

Note: Register function active at the falling edge of VSD except STBYB, RESETB register bits.

Registers list below require Vsync trigger:

DITHB, CFTYP, FPOL, VSET, UPDN, SHLR, DDLY, HDLY, INVSL, CON, BRI, HUE, SAT, SCONB, SCONR, SBRIR, SBRIB

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R03: Input Data Format Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	DENPOL	1b	R/W	DEN input pin polarity control. DENPOL="0", DEN negative polarity. DENPOL="1", DEN positive polarity. (Default mode)
Bit[6]	CLKPOL	0b	R/W	CLKIN pin polarity control. CLKPOL="0", CLKIN negative edge latch data. CLKPOL="1", CLKIN positive edge latch data. (Default mode)
Bit[5]	HSDPOL	0b	R/W	HSD pin polarity control. HSDPOL="0", HSD negative polarity. (Default mode) HSDPOL="1", HSD positive polarity.
Bit[4]	VSDPOL	0b	R/W	VSD pin polarity control. VSDPOL="0", VSD negative polarity. (Default mode) VSDPOL="1", VSD positive polarity
Bit[3:0]	SEL[3:0]	1100b	(R) R/W	Input data format selection. Note: Different SEL[3:0] setting resolution in different AC timing.

SEL [3:0]: Data input mode

SEL3	SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	0	CCIR601 YUV 1280 input format（YUV mode A）	24.54MHz
0	0	0	1	CCIR601 YUV 1280 input format（YUV mode B）	24.54MHz
0	0	1	0	CCIR601 YUV 1440 input format（YUV mode A）	27MHz
0	0	1	1	CCIR601 YUV 1440 input format（YUV modeB）	27MHz
0	1	0	0	CCIR656 YCbCr input format（YCbCr mode A）	27MHz
0	1	0	1	CCIR656 YCbCr input format（YCbCr modeB）	27MHz
0	1	1	0	-	-
0	1	1	1	-	-
1	0	0	0	8-bit digital RGB input format HV Mode (NTSC only)	27MHz
1	0	0	1	8-bit digital RGB input format DE Mode (NTSC only)	27MHz
1	0	1	0	8-bit digital RGB through mode input format HV Mode (NTSC only)	27MHz
1	0	1	1	8-bit digital RGB through mode input format DE Mode (NTSC only)	27MHz
1	1	0	0	24-bit digital RGB input format HV Mode(NTSC only)	6.4MHz
1	1	0	1	24-bit digital RGB input format DE Mode(NTSC only)	6.4MHz
1	1	*	*	-	-

Note: Hsync and Vsync will be ignored in DE mode

Remark:RGB through mode will bypass 3-wire SWD[2:0] function; TCON will not arrange data color mapping.

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4. Optical Specifications

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing angle (CR≥ 10)		θ_L	Φ=180°(9 o'clock)	50	60	-	degree	Note 1
		θ_R	Φ=0°(3 o'clock)	50	60	-		
		θ_T	Φ=90°(12 o'clock)	40	50	-		
		θ_B	Φ=270°(6 o'clock)	50	60	-		
Response time		T_{ON}	Normal θ=Φ=0°	-	25	40	msec	Note 3
		T_{OFF}						
Contrast ratio		CR		250	300	-	-	Note 4
Color Chromaticity	White	W_X		0.260	0.310	0.360	-	Note 2 Note 5 Note 6
		W_Y		0.283	0.333	0.383	-	
	Red	R_X		0.574	0.624	0.674	-	
		R_Y		0.318	0.368	0.418	-	
	Green	G_X		0.300	0.350	0.400	-	
		G_Y		0.500	0.550	0.600	-	
	Blue	B_X		0.093	0.143	0.193	-	
		B_Y		0.069	0.119	0.169	-	
Luminance		L		360	410	--	cd/m^2	Note 6
Luminance uniformity		Y_U		75	80	--	%	Note 7

Test Conditions:

1. DV_{DD}=3.3V, I_L =20mA(Backlight current),the amblent temperature is 25℃.
2. The test systems refer to Note 2.

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Note 1: Definition of viewing angle range

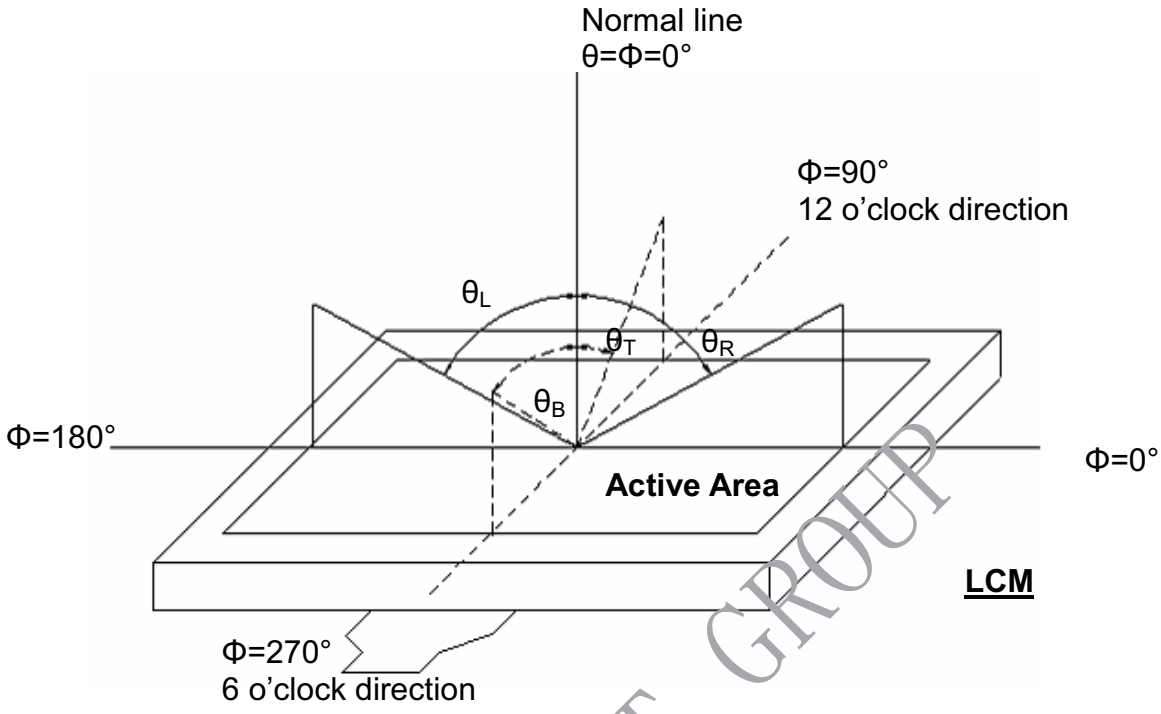

Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

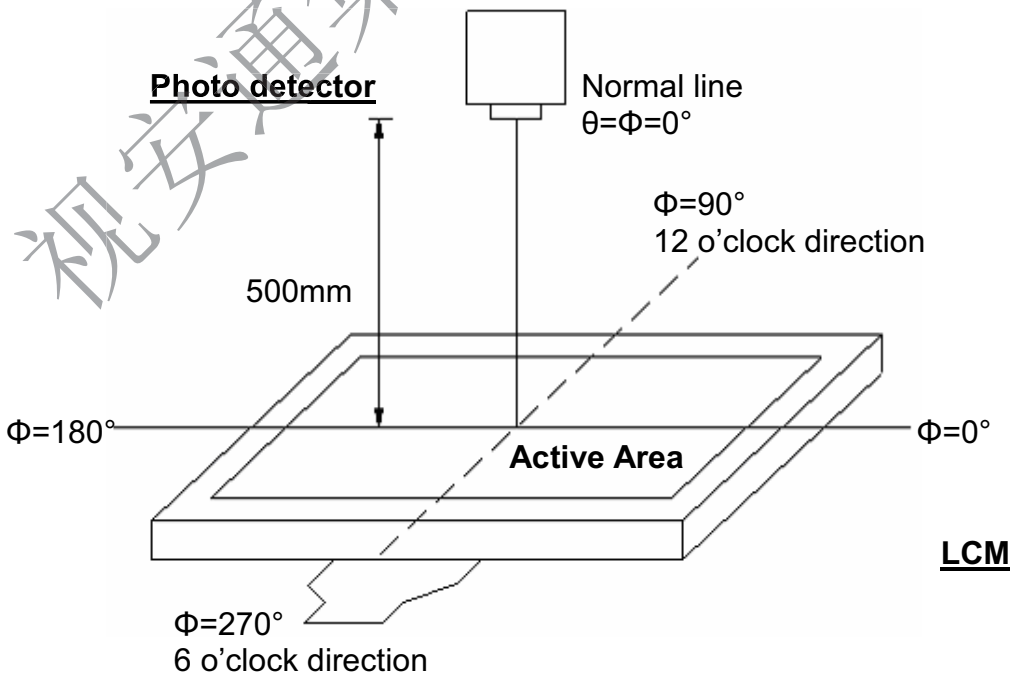

Fig. 4-2 Optical measurement system setup

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Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

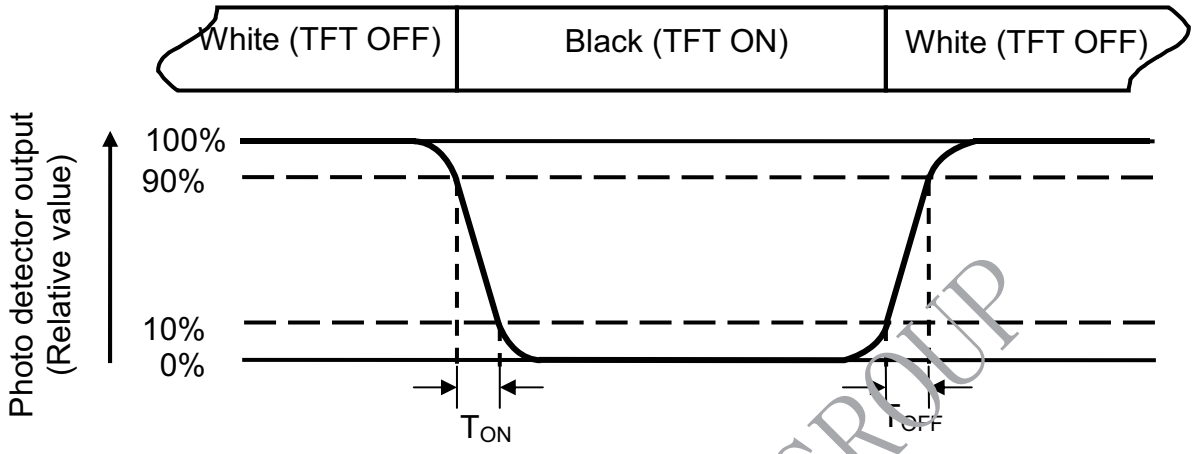

Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

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Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

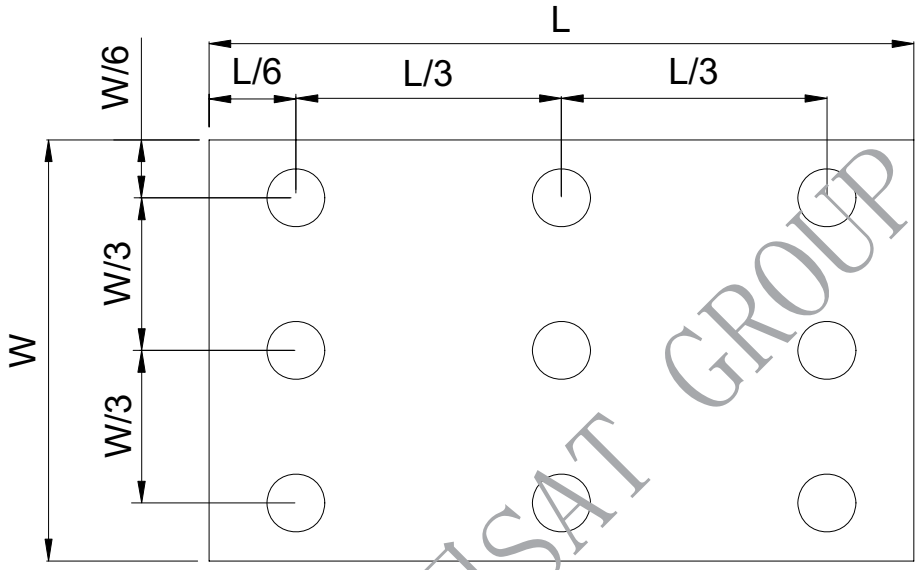

Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

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5. Reliability Test Items

(Note3)

Item	Test Conditions	Remark
High Temperature Storage	Ta = 80℃ 240hrs	Note 1，Note 4
Low Temperature Storage	Ta = -30℃ 240hrs	Note 1，Note 4
High Temperature Operation	Ts = 70℃ 240hrs	Note 2，Note 4
Low Temperature Operation	Ta = -20℃ 240hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH 240hrs	Note 4
Thermal Shock	-30℃/30 min ~ +80℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature.	Note 4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

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6. General Precautions

6.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

6.4. Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

6.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

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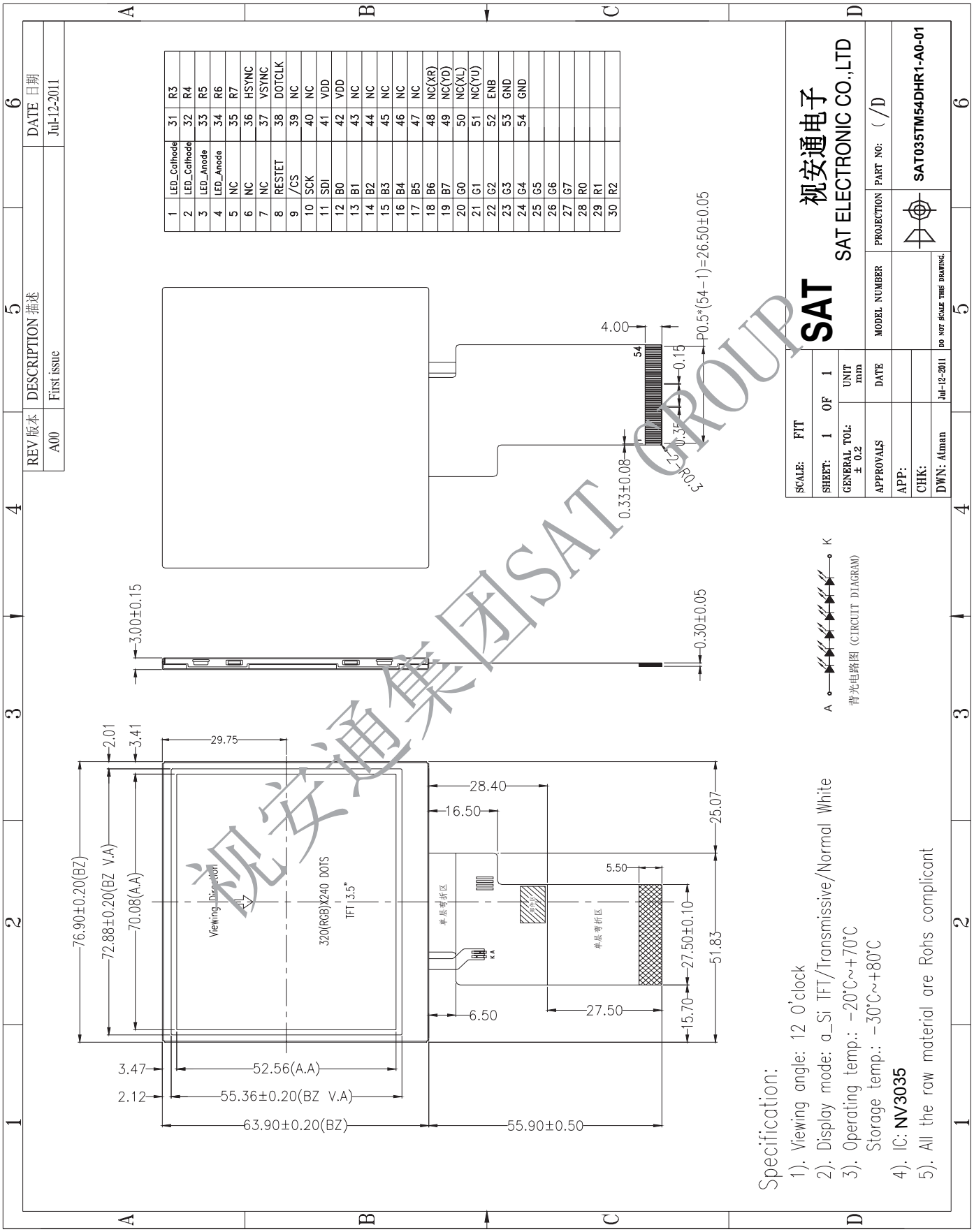
7. Mechanical Drawing



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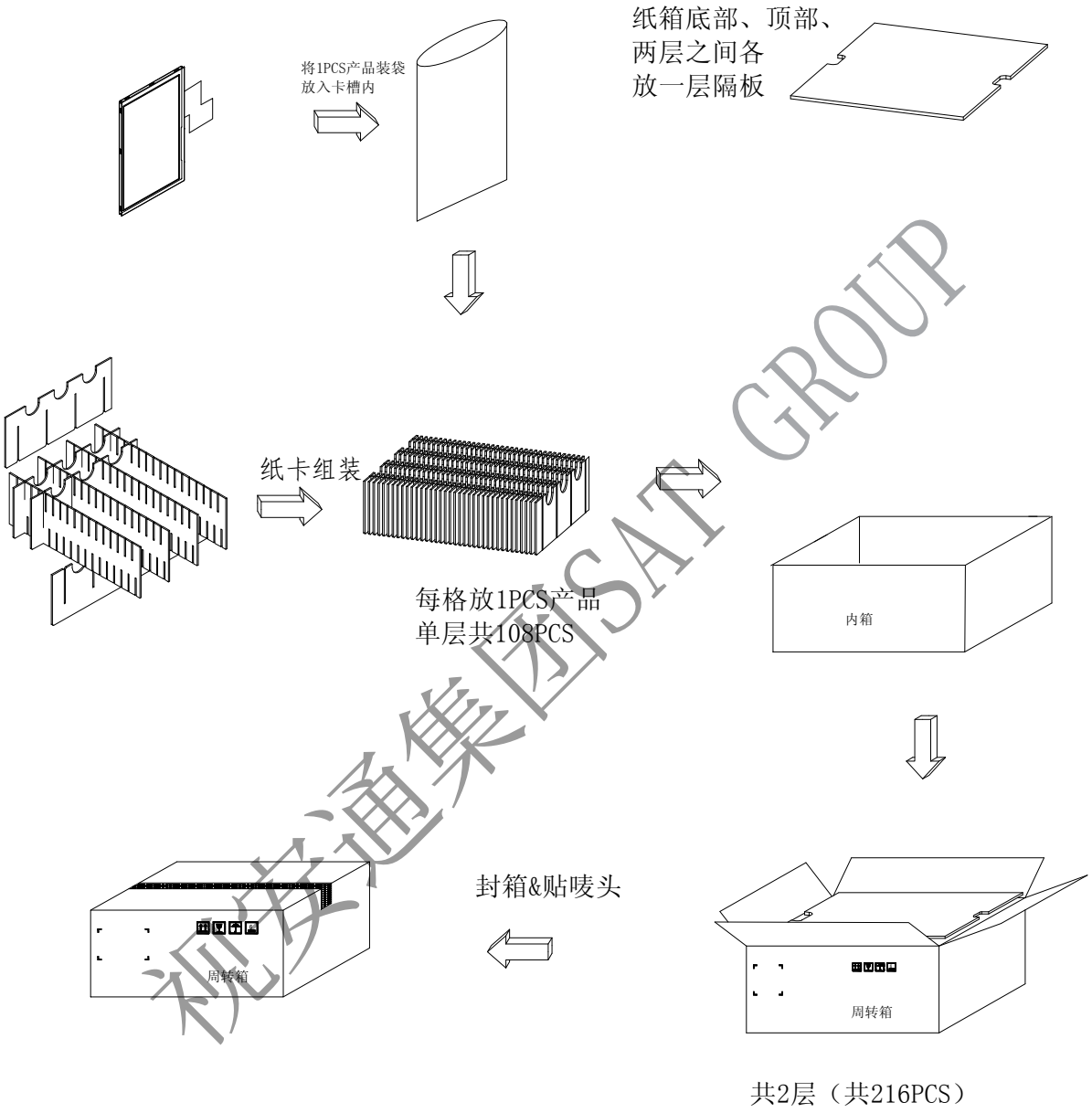
8. Package Drawing



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9 . Product ID Rule

Product Name

□□□ □□□ □□ — □□ □ □ — □□ □□□ — □□

(1) (2) (3) (4) (5) (6) (7) (8)(9) (10)

No	Definition	Specifications
(1)	TFT LCM Productor No.	SAT---- SAT ELECTRONIC CO.LTD
(2)	Display monitor opposite angle line size	Unit :inch or mmm (size <10 inch: takes two integers ; size >=10 inch: takes three integers)
(3)	LCD Type	AU----AUO ; CP----CPT ; PV----PVI ; TM----TIANMA ; HS----HSD ; LG----LG ; Wi----Wintek ; CM----CMO ; HY----Hydis ; HI----Hitach; Sh----Sharp ; BO---BOE 。。。
(4)	Interface PIN Number	By two figures characters expression from 01 to 99
(5)	Type	A---- Alternated Video Signal; D---- Data Video Signal;
(6)	LED Back Light Type	H----high light ; M---- Commonly light; L---- low light
(7)	LED Back Light colored warp	Rx----red ; Gx----green ; Bx---- blueness; Yx---- white; P----PVI; x---- warp distinction,1 minimal,9 maximal
(8)	BK Productor number	By The English litters : A 0~ Z9 A0---MeX

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No	Definition	Specifications
(9)	FPC Type	S---short L---Long
(10)	IC Type	By two figures characters expression from 01 to 99

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